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DESCRIPTION

SEMICONDUCTOR PACKAGE AND STACKED SEMICONDUCTOR PACKAGE

5 TECHNICAL FIELD

The present invention relates to thin semiconductor packages and three-dimensionally stacked semiconductor packages, and more particularly, to a semiconductor package and a stacked semiconductor package with an improved package structure which 10 can facilitate packaging of semiconductor devices regardless of the number of input/output leads thereof.

BACKGROUND ART

Figs. 22 through 25 are sectional views showing the 15 conventional semiconductor packages described in Japanese Patent Laid-Open Publication No. Hei 8-335663. The semiconductor device shown in Fig. 22 is constructed such that electrode pads 504 of an interposer substrate 502 which has a patterned wiring 505 and an insulating film 510 laminated on both surfaces of the 20 patterned wiring 505 are connected to the electrodes of a semiconductor chip 501 via conductors 503. Then, an insulating resin 509 is inserted in between the interposer substrate 502 and the semiconductor chip 501. Subsequently, the interposer substrate 502 is folded from the side surfaces to the rear 25 surface of the semiconductor chip 501, and the insulating resin 509 is applied to an area of the rear surface of the semiconductor chip 501 at which the chip surface is exposed, thereby adhering the interposer substrate 502 to the

semiconductor chip 501. This allows for obtaining a small semiconductor package which has generally the same size as that of a bare chip of the semiconductor chip 501. In this semiconductor device, the interposer substrate 502 is adhered to 5 a surface of the semiconductor chip 501 using the insulating resin 509 which serves as an adhesive.

Fig. 23 shows a small three-dimensional semiconductor device which is constructed by stacking the semiconductor device shown in Fig. 22 in layers using solder bumps 507 as a coupling 10 material, and has generally the same size as that of the bare chips.

Fig. 24 is a cross-sectional view showing the above-noted three-dimensional semiconductor devices packaged on a mother board substrate 511.

15 Additionally, Fig. 25 shows an underfill resin 508 filled around the solder bumps 507 that connect between the mother board substrate 511 of the three-dimensional semiconductor device packaged thereon and the lowermost stage semiconductor device.

20 Figs. 26 to 29 are cross-sectional views showing other conventional semiconductor devices described in Japanese Patent Laid-Open Publication No. 2001-196504. The semiconductor device is constructed such that electrode pads 504 of a flexible interposer substrate (flexible substrate) 506 which has a patterned wiring 505 and a thermoplastic insulating resin 512 25 laminated on both surfaces of the patterned wiring 505 are connected to the electrodes of a semiconductor chip 501 via conductors 503. While being heated, the flexible interposer substrate (flexible substrate) 506 is then bent to be adhered to

the side and rear surfaces of the semiconductor chip, thereby forming a small semiconductor package having generally the same size as that of the bare chip.

This semiconductor device is totally different from the 5 one shown in Fig. 22 in using the thermoplastic resin as an insulator for the interposer substrate. Since the interposer substrate 506 itself has an adhesive property and is reduced in elastic modulus when heated, the process of bending the substrate to be adhered to the chip is more simplified than that for the 10 semiconductor device shown in Fig. 22.

On the other hand, Fig. 27 illustrates a small three-dimensional semiconductor device which is constructed by stacking the semiconductor device shown in Fig. 26 in layers using the solder bumps 507 to have generally the same size as that of the 15 bare chips.

Fig. 28 shows the three-dimensional semiconductor device packaged on the mother board substrate 511, and Fig. 29 shows the insulating resin 509 filled in between the lowermost stage semiconductor package and the mother board substrate 511.

20 By using a thin interposer substrate 502, the semiconductor package shown in Fig. 22 can be formed into a semiconductor package having generally the same size as that of the semiconductor device. Decreasing the package size is effective means for providing an increased packing density, and 25 thus this package structure can be one of the effective means for forming small packages.

Furthermore, this package can be provided with the electrode pad 504 on the front and rear surfaces. Also, outer

bumps 1a, 1b can be formed on the pads 504 like as a package shown in Fig. 20, thereby enabling not only planar packaging on a mother board substrate 7 but also three-dimensional packaging thereon by staking packages one on another like as a package 5 shown in Fig. 21. The same semiconductor devices can be packaged in the packaging structure as shown in Fig. 27, thereby enabling high packing density packaging.

However, the conventional semiconductor package has a package structure that can provide a reduced planar packaging 10 area and enables packaging at much higher packing densities through the three-dimensional packaging, but with some limitations. As described above, the same semiconductor devices or semiconductor devices having the same outer dimensions can be formed one on another in the three-dimensional packaging 15 structure as shown in Fig. 27. However, as shown in Fig. 21, for the three-dimensional packaging of semiconductor devices having different outer dimensions, it is desirable for upper stage semiconductor packages 301a, 301b, 301c to have the same 20 dimensions or to be reduced in size with respect to the lowermost stage semiconductor package 301d. This imposes a restriction on the order in which the semiconductor devices can be stacked in layers. The outer bump 1a serving for connection between packages can be located at the center of the package to provide a higher degree of flexibility to the order of stacking the 25 packages according to their dimensions. However, this is not desirable in terms of ensuring the stability in packaging. It is also conceivable that the outer bump of an upper semiconductor package cannot be accommodated within the dimensions of its lower

semiconductor package. Significant increases in number of input/output leads of semiconductor devices may cause the electrode pad of an upper semiconductor device to be placed with difficulty at a connectable area of its smaller lower 5 semiconductor package. Even when this is possible, an extremely fine wiring pattern would be required, thus resulting in a very expensive semiconductor package, which is not preferable. This problem with patterning would occur not only in the case where a lower semiconductor package is less in size than the upper 10 semiconductor package but also in some other cases. When a semiconductor device with a large number of input/output leads is redesigned to have a wiring density enough for package-level packaging, such a case would occur in which a relocated electrode pad can not be accommodated within the area of the semiconductor 15 device. This problem would affect the design rule for the interposer substrate responsible for re-patterning of wirings, and thus an out of spec design would have serious effects on manufacturing costs, which is not preferable.

As a solution to address these problems, the package may 20 be conceivably increased in size relative to the semiconductor device. This seems to be against a feature that the package can be made generally in the same size as that of the semiconductor device. However, the package structure shown in Fig. 20 also has a feature that the package can be reduced in thickness. It can 25 be effective means for high density packaging that the package is increased in area up to the necessary but least possible level for three-dimensional packaging of thin packages.

On the other hand, as means for reducing manufacturing

costs for semiconductor devices, such a technique is employed in which their outer dimensions are reduced to provide an increased number of devices per wafer. For the semiconductor package shown in Figs. 20 and 21, such a change in design would require a 5 modification in design of a flexible substrate 101 which has been designed for each of the semiconductor packages 301a, 301b, 301c, and 301d. Furthermore, even when some of the semiconductor devices have been changed, the flexible substrate to be used for the semiconductor package present above or below them need to be 10 changed in design.

Also as a method to address such a problem, packages are desirably standardized in size independent of semiconductor devices, e.g., in a fixed size or by providing the electrode pad at a predetermined location. To this end, such a structure is 15 also desired which allows the package to be greater in size than the semiconductor device.

On the other hand, when a semiconductor device with a large number of input/output leads is re-patterned to have a wiring density enough for package level packaging, a re-patterned 20 electrode pad can be accommodated within the area of the semiconductor device. However, in some cases, the re-patterning of wirings may be performed in a single layer with difficulty. Conventionally, the flexible substrate with an insulating film laminated on both surfaces of a patterned wiring has a patterned 25 wiring portion formed in a single layer. A low wiring density would enable patterning in a single layer. However, when input/output leads are arranged in a grid pattern at an increased wiring density with an increased number of leads allocated to one

side of the grid pattern, some patterning arrangements may be or may not be realized. This causes some restrictions to be imposed on the arrangement. It is thus desired a method for addressing these problems to provide a higher degree of flexibility to the 5 flexible substrate to be employed.

DISCLOSURE OF THE INVENTION

It is therefore an object of the present invention to provide a semiconductor package and a three-dimensional stacked 10 semiconductor package which allow the outer dimensions of the semiconductor package and the design flexibility of re-patterning of wirings to be independent of the semiconductor device, thereby facilitating three-dimensional packaging.

A semiconductor package according to the present invention 15 has a semiconductor device with one or more electrodes being formed on a circuit-bearing surface and a flexible substrate with a thermoplastic insulating layer on either or both sides of a patterned wiring. An electrode provided on the flexible substrate is connected to the electrode of the semiconductor 20 device and sealed by the thermoplastic insulating layer. The flexible substrate is bent, and an electrode can be provided on the electrode-bearing surface and another surface. The semiconductor package is characterized in that the flexible substrate has at least two or more layers of circuit patterns 25 formed thereon.

In this semiconductor package, it is preferable to form a groove or a portion having less number of wiring layers at a bend of the flexible substrate or on a region including the bend. It

is also possible to construct the semiconductor package such that a cavity is formed on the flexible substrate so as to accommodate the semiconductor device in the cavity portion.

A semiconductor package according to another aspect of the present invention has a semiconductor device with one or more electrodes being formed on a circuit-bearing surface, and a flexible substrate with a thermoplastic insulating material on either or both sides of a patterned wiring. An electrode provided on the flexible substrate is connected to the electrode of the semiconductor device and sealed by the thermoplastic insulating material. The flexible substrate is bent, and an electrode can be provided on the electrode-bearing surface and another surface. The semiconductor package is characterized in that the bent flexible substrate includes portions directly adhered to each other.

In this semiconductor package, a semiconductor device can be accommodated in a recessed portion created by the flexible substrates being bent and directly adhered to each other.

A stacked semiconductor package according to the present invention is characterized in that a plurality of the aforementioned semiconductor packages according to the present invention are three-dimensionally stacked in layers and electrically connected to each other via the electrode. In this case, the plurality of semiconductor packages may be either the same in structure or a plurality of semiconductor packages of different structures being stacked in layers.

To address the aforementioned problems, the present invention employs a flexible substrate, used for semiconductor

packages, which has at least two or more layers of patterned wiring formed thereon. The flexible substrate having two or more layers of patterned wiring formed thereon is bent along the outer shape of the semiconductor device. To facilitate the bending, 5 the bends are provided with a groove or a thin layer portion with a reduced number of wiring layers formed thereon.

Such a structure is introduced in which a cavity is formed on the flexible substrate, as means for reducing an increase in thickness of the flexible substrate caused by a plurality of 10 wiring layers being introduced onto the flexible substrate, i.e., an increase in thickness of the semiconductor package.

Alternatively, to freely select the outer dimensions of the semiconductor package, such a structure is introduced which allows the bent flexible substrate has portions which are 15 directly adhered to each other.

The semiconductor package according to the present invention allows for freely designing the outer dimensions and the arrangement of outer bumps serving to connect between semiconductor packages as well as for packaging different types 20 of semiconductor devices having different dimensions and a different number of input/output leads for three-dimensional packaging.

That is, the semiconductor package and the stacked semiconductor package according to the present invention allow a 25 plurality of semiconductor devices to be accommodated in a package reduced in thickness as well as to be stacked in layers for three-dimensional packaging without being restricted by the number of input/output leads and the outer dimensions of the

semiconductor device. Furthermore, the present invention makes it possible to standardize the package size and the outer bump position.

5 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional view showing a semiconductor package according to a first embodiment of the present invention;

Fig. 2 is a perspective view showing a manufacturing step of a flexible substrate;

10 Fig. 3 is a cross-sectional view also showing a manufacturing step of a flexible substrate;

Fig. 4 is a cross-sectional view also showing a manufacturing step of a flexible substrate;

15 Fig. 5 is a cross-sectional view also showing a manufacturing step of a flexible substrate;

Fig. 6 is a cross-sectional view showing a flexible substrate;

Fig. 7 is a cross-sectional view also showing a flexible substrate;

20 Fig. 8 is a cross-sectional view also showing a flexible substrate;

Fig. 9 is a cross-sectional view showing an assembly step of a semiconductor package according to a second embodiment of the present invention;

25 Fig. 10 is a cross-sectional view showing a semiconductor package according to the second embodiment of the present invention;

Fig. 11 is a cross-sectional view showing an assembly step

of a semiconductor package according to a third embodiment of the present invention;

Fig. 12 is a cross-sectional view showing a semiconductor package according to the third embodiment of the present invention;

Fig. 13 is a cross-sectional view showing an assembly step of a semiconductor package according to a fourth embodiment of the present invention;

Fig. 14 is a cross-sectional view showing a semiconductor package according to the fourth embodiment of the present invention;

Fig. 15 is a cross-sectional view showing a stacked semiconductor package having this semiconductor package stacked in layers;

Fig. 16 is a cross-sectional view showing an assembly step of a semiconductor package according to a fifth embodiment of the present invention;

Fig. 17 is a cross-sectional view showing a semiconductor package according to the fifth embodiment of the present invention;

Fig. 18 is a cross-sectional view showing an assembly step of a semiconductor package according to a sixth embodiment of the present invention;

Fig. 19 is a cross-sectional view showing a stacked semiconductor package using the semiconductor package according to the sixth embodiment of the present invention stacked in layers;

Fig. 20 is a cross-sectional view showing a semiconductor

package;

Fig. 21 is a cross-sectional view showing a stacked semiconductor package having the semiconductor package stacked in layers;

5 Fig. 22 is a cross-sectional view showing a conventional semiconductor package;

Fig. 23 is a cross-sectional view showing the conventional semiconductor package stacked in layers;

10 Fig. 24 is a cross-sectional view showing the stacked semiconductor package being packaged on a mother board substrate;

Fig. 25 is a cross-sectional view showing an underfill resin being filled;

Fig. 26 is a cross-sectional view showing another conventional semiconductor package;

15 Fig. 27 is a cross-sectional view showing the conventional semiconductor package stacked in layers;

Fig. 28 is a cross-sectional view showing the stacked semiconductor package being packaged on a mother board substrate; and

20 Fig. 29 is a cross-sectional view showing an insulating resin being filled.

BEST MODE FOR EMBODYING THE INVENTION

Now, embodiments of the present invention will be described below more specifically with reference to the accompanying drawings. Fig. 1 is a cross-sectional view showing a semiconductor package 301 according to the embodiment. There are one or more electrodes formed on a circuit-bearing surface of

a semiconductor chip 6, around which a flexible substrate 101 is placed. The flexible substrate 101 is provided with a pair of wirings 3 formed on the front and rear surfaces of an insulating layer 5, and the outsides of the wirings 3 are also coated with 5 thermoplastic resin layers 4. Instead of the thermoplastic resin layer 4 placed outside the flexible substrate 101, an insulating layer formed of an ordinary insulating material similar to that of the insulating layer 5 may also be placed. The pair of wirings 3 are connected through via holes 9 formed in the 10 insulating layer 5. The inner wiring 3 on the flexible substrate 101 is connected to an inner bump 2 of the semiconductor chip 6, while an electrode pad 8 formed on the outer wiring 3 is connected with an outer bump 1. The inner bump 2 is sealed within the thermoplastic resin layer 4 formed of a thermoplastic 15 insulating resin. The flexible substrate 101 is bent around the semiconductor chip 6 and provided with electrodes formed on a surface aligned with the electrode-bearing surface of the semiconductor chip 6 and at a predetermined position on another surface. The wirings 3 of the flexible substrate 101, which 20 constitute the circuit pattern, may be not only of two layers as in the aforementioned embodiment but also of multi-layers such as three layers or more.

The flexible substrate 101 and the semiconductor chip 6 are connected to each other via the inner bump 2 which is pre-formed 25 on the electrode of the semiconductor chip 6. At this time, the thermoplastic resin layer 4 formed on a surface of the flexible substrate 101 in contact with the semiconductor chip 6 is heated when connected, thereby allowing the connection to be

sealed with the thermoplastic resin at the same time as the connection. In addition, the flexible substrate 101 can be bent along the semiconductor chip 6 while being heated, thereby facilitating the formation of the semiconductor package 301.

Now, an explanation is given to how the flexible substrate 101 is formed. This flexible substrate 101 is different from the flexible substrate shown in Fig. 1 in that a bend or an area including the bend is a groove or a thin layer portion 102 having a reduced number of wiring layers. The flexible substrate 101 is formed such that an insulating resin sheet 14 is affixed to a metal foil 10 as shown in Fig. 2, and then as shown in Fig. 3, the metal foil 10 is etched to form patterned wirings 11, outer pads 12, and inner pads 13, and then a plurality of insulating resin sheets 14 on which the patterned wirings 11 et al. are formed are affixed to each other. Those openings which are provided on the insulating resin sheet 14 at the positions aligned with the inner pads 13 and the outer pads 12 may be pre-formed on the insulating resin sheet 14 or may be formed after the insulating resin sheet 14 and the metal foil 10 are affixed to each other. The methods for forming the openings include etching, laser processing, or machining such as punching. A photosensitive resin may be used as an insulating resin sheet 14. In this case, the openings can be formed by photolithography. However, in terms of processing accuracy and costs, the openings are desirably formed using laser processing.

When wirings are formed in a single layer on the flexible substrate 101, the flexible substrate is formed of a thin thermoplastic resin layer, a metal foil to serve as a wiring

layer, and a thin insulating resin layer or a thin thermoplastic resin layer. This facilitates bending and adhesion of the flexible substrate when heated and bent. The metal foil serving as a wiring layer can be formed of a metal such as copper, gold, 5 or aluminum, or any other metals so long as they are electrically conductive; however, copper which is inexpensive but has a high electrical conductivity and good machinability is preferably employed. The processing to the metal foil can be done to the metal foil of a thickness on the order of several hundreds of 10 micrometers. However, the foil of a thickness of 38 μm , 18 μm , 10 μm , or 5 μm preferably facilitates bending and makes an assembled semiconductor package thinner. On the other hand, the processing to the thermoplastic resin layer and the insulating resin layer can be done to the thermoplastic resin layer and the 15 insulating resin layer of a thickness on the order of several hundreds and tens of micrometers. However, a thickness of 50 μm or less can preferably facilitate bending and makes an assembled semiconductor package thinner. Preferably a thickness of 25 μm or less, more preferably 10 μm or less, will be advantageous in 20 making the package thinner. The thermoplastic resin may be any resin such as polyimide, polyamide, epoxy, or silicone resin so long as they have thermoplastic property, or a combination thereof. The thermoplastic resin is desirably composed predominantly of polyimide in terms of heat resistance and 25 machinability.

To form a number of wirings on the flexible substrate 101, a thermoplastic resin should be used for the insulating resin layer to facilitate bending, and both the insulating resin layer

and the metal foil layer are desirably made as thin as possible. However, in terms of ensuring stability in manufacturing the flexible substrate and reducing manufacturing costs, a groove or a portion having a different number of wiring layers is formed at 5 a portion of the flexible substrate to be bent or at an area containing the portion to be bent. That is, a portion contributing to bending is made in a single layer or a nearly single layer, thereby facilitating the bending. Alternatively, a multi-layered wiring portion is prepared only for a portion 10 requiring re-patterning of wirings, with the other portions containing the bend being made in a single layer or a nearly single layer.

As described earlier, the flexible substrate 101 is formed by the insulating resin sheet 14 and the metal foil 10 being 15 affixed to each other. Here, as shown in Fig. 4, in a step after the patterned wirings 11 or the like have been formed, the insulating resin sheets 14 having punched portions 15 pre-formed can be affixed to each other, thereby forming such groove portions. As shown in Fig. 5, after these grooves have been 20 formed, the flexible substrate 101 is cut at appropriate cutting portions 17, thereby completing the flexible substrate 101 easy to bend.

The combination of these grooves, the wirings 3 processed appropriately, the thermoplastic resin layer 4 and the insulating 25 resin layer 5 makes it possible to form the structures as shown in Figs. 6 through 8. Fig. 6 shows the grooves 102 formed in the upper thermoplastic resin layer 4, Fig. 7 showing the grooves 102 formed in the upper thermoplastic resin layer 4 and the

intermediate insulating resin layer 5, and Fig. 8 showing the grooves 102 formed in the upper thermoplastic resin layer 4 and the lower thermoplastic resin layer 4.

On the other hand, the same processing method can be
5 applied to the formation of grooves at the bends as well as to
the formation of a cavity at the portion in which the
semiconductor chip 6 is connected, thereby forming a structure in
which the semiconductor chip 6 is embedded in the cavity defined
in the flexible substrate 101.

10 Figs. 9 and 10 are cross-sectional views showing a second
embodiment of the present invention. As shown in Figs. 6 and 7,
Fig. 9 is a cross-sectional view showing a step of forming a
semiconductor package using the flexible substrate 102 having
grooves formed in the thermoplastic resin layer 4 and the wiring
15 3 at one surface of the flexible substrate 102, and Fig. 10 is a
cross-sectional view showing a semiconductor package after having
been assembled. The flexible substrate 101 shown in Figs. 9 and
10 is constructed such that two insulating layers 5 are formed on
the both sides of a wiring 3 centered therebetween, and other two
20 wirings 3 are then laminated on the both outsides of the
insulating layers 5, and thermoplastic resin layers 4 are
laminated on the outsides of the outside wirings 3, with the
wiring layers arranged in three layers. The thermoplastic resin
layer 4 on the lower surface of the flexible substrate 101, the
25 two layers of wiring 3, and the middle wiring 3 are partially
removed at the side portions below the lower surface of the
semiconductor chip 6. The removed portions are thin layer
portions 102 where only the thermoplastic resin layer 4, the

wiring 3, and the insulating layer 5 are present. As illustrated with arrows Y1 and Y2 in Fig. 10, the flexible substrate 101 is folded to bring the uppermost thermoplastic resin layer 4 into contact with the side and upper surfaces of the semiconductor 5 chip 6, thereby fabricating the semiconductor package 301. In this semiconductor package 301, the flexible substrate 101 on the side surfaces thereof has the thin layer portions 102 being half in thickness the portion on the lower surface of the semiconductor chip 6, thereby facilitating bending even at the 10 portions such as the side surfaces of the semiconductor chip 6 where more force is required for bending.

Now, by way of example, an explanation is given to how the semiconductor package shown in Figs. 9 and 10 is fabricated. For example, memory LSIs of three types having different dimensions 15 and a logic LSI of one type are prepared as semiconductor devices. For example, the memory LSIs have outer dimensions of about 5mm to 10mm with about 50 input/output pins, while the logic LSI has outer dimensions of about 10mm with about 400 input/output pins. For example, the LSIs are polished to a thickness of 50 μm and a 20 gold bump is formed on each of the input/output leads.

For example, as the flexible substrate, prepared is a substrate which has a copper foil of 18 μm in thickness, and a thermoplastic polyimide of about 20 μm in thickness is formed on the front and rear surfaces of the copper foil. The portions to 25 which the inner and outer bumps are connected are provided holes bored in the thermoplastic polyimide by laser processing and subjected to typical various pre-processing, and then plated with Ni and Au as a barrier metal.

Although the flexible substrate for use with the memory LSI is formed in a single layer, the flexible substrate 101 for use with the logic LSI is provided with wirings in three layers as shown in Figs. 9 and 10. Furthermore, the flexible substrate 101 for use with the logic LSI is provided with grooves and thereby single layers or the thin layer portions 102 on the portions serving as the bends when the flexible substrate 101 is bent along the outer circumference of the semiconductor chip 6.

First, the LSIs are mounted on the flexible substrate, in the case of which an ordinary flip chip mounter can be used. The flexible substrate is fixed on a stage which can be heated, by vacuum adhesion, and the LSIs are aligned using a camera to be mounted thereon. During the mounting, pressure and heat are simultaneously applied to joint the Au bumps to the electrode pads of the flexible substrate. The heating is carried out at a temperature enough for the thermoplastic polyimide to start flowing, thereby allowing for joining the Au bump portions as well as sealing the joints.

Subsequently, the flexible substrate 101 is bent along the outer circumference of the semiconductor chip 6, thereby forming the semiconductor package 301. The flexible substrate is bent along one side of the semiconductor chip 6, and fixedly pressed against the opposite surface of the semiconductor chip 6 using a sufficiently heated jig. The flexible substrate for use with the logic LSI, which is provided in advance with the thin layer portions 102 at the bends, can be bent in the same manner as the package for memory LSIs.

After the flexible substrate has been sufficiently cooled

down, the sample is taken out of the stage of the flip chip mounter, flux is applied to the electrode pads for the outer bumps pre-formed on the outer circumference portion, and then solder balls 1a, 1b are mounted thereon. For example, SnPb 5 eutectic solder balls of 0.3mm in diameter can be used; however, solders other than SnPb-based ones or Pb-free solders such as Sn-Ag and Sn-Zn based solders may also be used. After the solder balls have been mounted, the sample is dipped into a reflow furnace, thereby forming the solder bumps (outer bumps) on the 10 semiconductor package. After having been dipped into the reflow furnace, the semiconductor package is cleaned and dried.

Four semiconductor packages thus fabricated are stacked in layers and allowed through the reflow step, thereby providing a three-dimensionally packaged stacked semiconductor package. 15 Although the logic LSI has as many as 400 input/output pins and requires external terminals to be formed in a 0.5mm-pitch complete area array, the semiconductor package thus obtained enables packaging generally in the same size as the outer dimensions of the LSI. The four semiconductor packages can also 20 be packaged three-dimensionally.

Figs. 11 and 12 are cross-sectional views showing a third embodiment of the present invention. The semiconductor package according to the third embodiment is constructed in the same manner as the aforementioned second embodiment but different in 25 the following two points. One is that the flexible substrate 101 is provided with the three-layer wiring structure left at the portion to which the semiconductor chip 6 is provided and all the other portions than this portion are provided with the thin layer

portions 102 all of which have a single-layer wiring. The other
is that the solder balls 1a provided on both the ends of the
flexible substrate 101 are directly connected to the wiring in
the uppermost layer (a single layer) but not to the wiring in the
5 lowermost layer of the three layers. The flexible substrate 101
also has the thin layer portions 102 at the bends on the sides of
the semiconductor chip 6, thereby being readily bent.

Now, by way of example, an explanation is given to how the
semiconductor package having this structure is fabricated. A
10 memory LSI of one type and a logic LSI of one type are prepared
as semiconductor devices. The memory LSI has outer dimensions of
about 5mm × 10mm with about 50 input/output pins, while the
logic LSI has outer dimensions of about 10mm × 100mm with about
200 input/output pins. Each of the LSIs is polished to a
15 thickness of 50 μm with a gold bump being formed on each of the
input/output leads.

As the flexible substrate, prepared is a substrate which
has a copper foil of 18 μm in thickness, on the front and rear
surfaces of which formed is a thermoplastic polyimide of about 20
20 μm in thickness. The thermoplastic polyimide at the portions to
which the inner and outer bumps are connected are provided with
holes bored therethrough by laser processing and subjected to
ordinary various pre-processing, and then plated with Ni and Au
as a barrier metal.

25 Although the flexible substrate for use with the memory
LSI is formed in a single layer, the flexible substrate 101 for
use with the logic LSI is provided with three wiring layers as
shown in Figs. 11 and 12. Furthermore, in the flexible substrate

101 for use with the logic LSI, three wiring layers are formed only on the area to which the semiconductor chip 6 is packaged, while a single layer is formed on the other portion.

Like the embodiment shown in Figs. 9 and 10, the LSIs are 5 mounted on the flexible substrate and then the flexible substrate 101 is bent along the outer circumference of the semiconductor chip 6, thereby forming the semiconductor package 301. The flexible substrate 101 for use with the logic LSI has single layer bends, thereby being readily bent as in the case of the 10 memory LSI.

Outer bumps are also formed to stack semiconductor packages in layers. The two semiconductor packages thus obtained can have sufficient number of outer bumps disposed on the LSI packaging area for connections of wirings, though the logic LSI 15 has as many as 200 input/output pins. Furthermore, these semiconductor packages can be stacked in layers, thereby forming a three-dimensional package.

Now, a fourth embodiment of the present invention will be described. Figs. 13 to 15 are cross-sectional views showing a 20 semiconductor package according to the fourth embodiment. This semiconductor package has a semiconductor device and a flexible substrate having a thermoplastic insulating material on either or both sides of a patterned wiring. The semiconductor package allows the electrode provided on the flexible substrate to be 25 connected to a predetermined electrode of the semiconductor device and sealed by the thermoplastic insulating material, the flexible substrate to be bent, and electrodes to be formed on the electrode-bearing surface and another surface. The semiconductor

package is characterized in that a flexible substrate has portions which are directly adhered to each other when the flexible substrate is bent.

That is, the flexible substrate 101 is bent along the 5 outer circumference portion of the semiconductor chip 6, thereby making it possible to fabricate the semiconductor package 301 having generally the same outer dimensions as those of the semiconductor chip 6. However, the flexible substrate 101 is bent at predetermined positions (X1, X2) off the outer dimensions 10 of the semiconductor chip 6, thereby affixing the portions of the flexible substrate 101 to each other via the thermoplastic resin layers 4.

This package structure has a demerit that the outer dimensions are greater than those of the semiconductor chip 6. 15 However, it still provides a thin semiconductor package and makes it possible to form a large number of electrode pads 8b on the lower surface of the semiconductor package. That is, this embodiment provides a merit of being available for semiconductor devices having high input/output pin counts. Furthermore, a 20 plurality of such semiconductor devices can be packaged for three-dimensional packaging regardless of the outer dimensions of the semiconductor devices and the input/output pin counts.

Such a semiconductor package can be formed such that the semiconductor chip 6 is connected to the flexible substrate 101, 25 and then the outer circumference portion thereof is bent in the directions Y1 and Y2 while the flexible substrate is being pressed at predetermined positions (X1, X2) and heated. It is also possible to bend the flexible substrate 101 in advance and

then mount the semiconductor chip 6 thereon.

Although the semiconductor package structures described above each can be used alone, a plurality of features can be incorporated into one semiconductor package upon manufacture.

5 The semiconductor packages thus fabricated can also be three-dimensionally packaged to form a stacked semiconductor package as shown in Fig. 15.

Now, by way of example, an explanation is given to how to fabricate the semiconductor package shown in Figs. 13 and 14.

10 The semiconductor package as shown in Figs. 13 and 14 is fabricated using a semiconductor chip 6 having outer dimensions of 5mm \times 5mm and the number of input/output leads of 100.

On the flexible substrate 101, the pads to which the semiconductor chip 6 is connected are formed on the thermoplastic resin bearing surface, and electrode pads 8a, 8b for use with outer bumps 1 are formed on the opposite surface. The electrode pad 8a is used with connection for three-dimensional packaging while the electrode pad 8b is used for packaging on the mother board 7. However, due to a large number of input/output leads, 20 the electrode pad 8b is disposed beyond the packaging area for the semiconductor chip 6.

Then, the semiconductor chip 6 is connected to the flexible substrate 101 via the inner bump 2 formed of gold bump pre-formed on the semiconductor chip 6. At this time, in the same method as shown in Figs. 9 and 10, the connection and sealing can be performed at the same time. The flexible substrate 101 is then fixed to a jig. The jig holds only the portion within between the predetermined bends X1 and X2 of the

flexible substrate 101 but not the outer circumference portion thereof. The outer circumference portions outside X1 and X2 which are not held are bent in the directions shown by arrows Y1 and Y2 using another jig, which can be heated, to be pressed 5 against and affixed to the flexible substrate 101 itself by being heated.

The bends X1 and X2 are designed in advance to stay at such positions as not to overlap the semiconductor chip 6, and can be shaped so that the semiconductor chip 6 is surrounded by 10 the flexible substrate 101 as shown in Fig. 14. For example, the wiring layer used for the flexible substrate 101 is a copper foil of 18 μm in thickness, with the resin layer being 20 μm in thickness. The semiconductor chip 6 can be made as thin as about 15 60 μm in thickness by polishing or the like to be thereby reduced approximately within the thickness to which the flexible substrate 101 is folded.

As shown in Fig. 15, the semiconductor package 301d thus obtained can be three-dimensionally packaged in conjunction with semiconductor packages 301a, 301b, 301c which are fabricated 20 using semiconductor chips 6a, 6b, 6c having larger outer dimensions in accordance with the outer dimensions, thereby forming a stacked semiconductor package 401.

Figs. 16 and 17 are cross-sectional views showing a semiconductor package according to a fifth embodiment of the 25 present invention. Referring to Figs. 16 and 17, an explanation is given to how the semiconductor package according to this embodiment is fabricated. The flexible substrate 101 having wirings stacked in layers is provided with the thin layer

portions 102 and a cavity 103 as shown in Fig. 16. For example, the wiring layer of the flexible substrate 101 is formed of a copper foil of about 20 μm in thickness, while each of the insulating resin layer 5 and the thermoplastic resin layer 4 is 5 formed in a thickness of about 20 μm . The thin layer portions 102 is adapted to have a single layer of wiring, while the cavity 103 is designed to suit the outer dimensions of the semiconductor chip 6 to be packaged.

In the same manner as in the first embodiment, the 10 semiconductor chip 6 reduced in thickness down to about 60 μm is connected and adhered to a predetermined position on the flexible substrate 101. Thereafter, the flexible substrate 101 is bent in the directions indicated by arrows Y1 and Y2 at the centers X1 and X2 of the thin layer portions 102. Upon being bent, the both 15 end parts of the flexible substrate 101 is held with a jig that can be heated, and adhered to the other parts of the flexible substrate 101 and the semiconductor chip 6 via the thermoplastic resin layers 4.

The semiconductor package 301 thus obtained can have the 20 large number of electrode pads 8a, 8b disposed on both the sides of the package for electrical connections, thereby making it possible to fabricate the semiconductor package 301 irrespective of the number of the input/output leads of the semiconductor chip 6. On the other hand, to package these semiconductor packages 25 three-dimensionally, it is possible to form a number of connection bumps on any semiconductor package to be packaged either at a lower or upper position. It is also possible to determine the outer dimensions of a package irrespective of the

outer dimensions of semiconductor devices, thereby realizing a package having a high degree of design freedom.

Now, referring to Fig. 18, a semiconductor package according to a sixth embodiment of the present invention will be 5 described. The flexible substrate 101 has the thin layer portions 102 at the bends and the cavity 103 at the packaging portion for a semiconductor chip 6a. Two semiconductor devices are packaged on the flexible substrate 101. The semiconductor chip 6a which is one of the semiconductor devices is packaged in 10 the cavity 103. This allows the other semiconductor chip 6b to be packaged on the same surface of the flexible substrate 101. The flexible substrate 101 is bent at the thin layer portions 102 and then adhered along the semiconductor chip 6b, thereby forming the semiconductor package 301.

15 The semiconductor package 301 thus obtained allows a larger number of electrode pads 8a, 8b to be formed on a multi-layered wiring area, thereby being three-dimensionally packaged via the outer bumps 1a, 1b formed on the existing electrode pads.

Fig. 19 is a cross-sectional view showing a stacked 20 semiconductor package according to a seventh embodiment of the present invention. A semiconductor package 301e includes a plurality of semiconductor devices shown in Fig. 18, and is configured such that the semiconductor package shown in Fig. 17 is mounted on the semiconductor package 301e, the semiconductor 25 package shown in Fig. 14 is further mounted thereon, and two stages of the semiconductor packages shown in Fig. 1 are still further mounted thereon. This three-dimensionally packaged semiconductor package is packaged on the mother board substrate 7.

The semiconductor packages according to the present invention can be combined in this manner to thereby fabricate a semiconductor package that can be three-dimensionally packaged regardless of the number of input/output leads and the outer 5 dimensions of the semiconductor devices.